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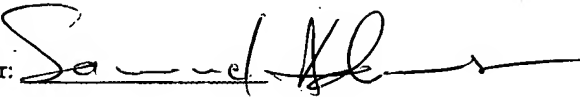
For: METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT
USING A SELECTIVE DISPOSABLE SPACER TECHNIQUE AND SEMICONDUCTOR
INTEGRATED CIRCUIT MANUFACTURED THEREBY

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
		6,043,537	3/28/2000	Jun, et al.		

Examiner:



Date Considered: 4/6/05